WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, said method comprising the steps of:

forming an insulating film being in contact with a semiconductor layer;

forming a gate electrode intersecting with the semiconductor layer through the insulating film; and

adding an impurity with one conductivity into the semiconductor layer through at least a portion of the gate electrode;

wherein an angle between a side of the gate electrode and the insulating film is in a range of 3 degrees to 60 degrees.

2. A method of fabricating a semiconductor device, said method comprising the steps of:

forming an insulating film being in contact with a semiconductor layer;

forming a gate electrode intersecting with the semiconductor layer through the insulating film;

first adding an impurity with one conductivity into the semiconductor layer through at least a portion of the gate electrode; and

second adding the impurity into the semiconductor layer without passing through the gate electrode;

wherein an angle between a side of the gate electrode and the insulating film is in a range of 3 degrees to 60 degrees.

3. A method of according to claim 2, wherein the impurity is added into the semiconductor layer using a mask covering the gate electrode and having a width wider than the gate electrode in a channel length direction in the second adding step.

4. A method of fabricating a semiconductor device, said method comprising the steps of:

forming an insulating film being in contact with a semiconductor layer;

forming a first conductive film being in contact with the insulating film;

forming a second conductive film being in contact with the first conductive film;

forming a gate electrode by patterning the first conductive film and the second conductive film;

wherein the gate electrode includes a first gate electrode and a second gate electrode being formed on the first gate electrode;

wherein the second electrode has a width narrower in a channel length direction than the first gate electrode; and

adding an impurity with one conductivity into the semiconductor layer through at least a portion of the first gate electrode;

wherein an angle between a side of the first gate electrode and the insulating film is in a range of 3 degrees to 60 degrees.

5. A method of fabricating a semiconductor device, said method comprising the steps of:

forming an insulating film being in contact with a semiconductor layer;

forming a first conductive film being in contact with the insulating film;

forming a second conductive film being in contact with the first conductive film;

forming a gate electrode by patterning the first conductive film and the second conductive film;

wherein the gate electrode includes a first gate electrode and a second gate electrode being formed on the first gate electrode;

wherein the second gate electrode has a width narrower in a channel length

direction than the first gate electrode;

first adding an impurity with one conductivity into the semiconductor layer by through at least a portion of the first gate electrode; and

second adding the impurity into the semiconductor layer without passing through the gate electrode;

wherein an angle between a side of the first gate electrode and the insulating film is in a range of 3 degrees to 60 degrees.

6. A method according to claim 5, wherein the impurity is added into the semiconductor layer using a mask covering the first gate electrode and having a width wider than the first gate electrode in a channel length direction.

7. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer the second semiconductor layer,

forming a second gate wiring on the first gate wiring;

first adding an n-type impurity into the first semiconductor layer by through at least a portion of the first gate wiring;

second adding the n-type impurity into the first semiconductor layer without passing through the first gate wiring; and

third adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks;

wherein an angle between a side portion intersecting with the first

semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

8. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer and the second semiconductor layer;

forming a second gate wiring on the first gate wiring;

first adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks;

second adding an n-type impurity into the first semiconductor layer through at least a portion of the first gate wiring; and

third adding the n-type impurity into the first semiconductor layer without passing through the first gate wiring;

wherein an angle between a side portion intersecting with the first semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

9. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer and the second semiconductor layer;

forming a second gate wiring on the first gate wiring;

first adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks;

second adding an n-type impurity into the first semiconductor layer without passing through the first gate wiring; and

third adding the n-type impurity into the first semiconductor layer through at least a portion of the first gate wiring;

wherein an angle between a side of a portion intersecting with the first semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

10. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer and the second semiconductor layer;

forming a second gate wiring on the first gate wiring;

first adding an n-type impurity into the first semiconductor layer through at least of the first gate wiring;

second adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks; and

third adding the n-type impurity into the first semiconductor layer without passing through the first gate wiring;

wherein an angle between a side portion intersecting with the first semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

11. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer and the second semiconductor layer;

forming a second gate wiring on the first gate wiring;

first adding an n-type impurity into the first semiconductor layer without passing through the first gate wiring;

second adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks; and

third adding the n-type impurity into the first semiconductor layer through at least a portion of the first gate wiring;

wherein an angle between a side portion intersecting with the first semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

12. A method of fabricating a semiconductor device including a CMOS circuit having an n-channel thin film transistor and a p-channel thin film transistor, said method comprising the steps of:

forming a first semiconductor layer and a second semiconductor layer;

forming an insulating film being in contact with the first semiconductor layer and the second semiconductor layer;

forming a first gate wiring intersecting with the first semiconductor layer and the second semiconductor layer;

forming a second gate wiring on the first gate wiring;

first adding an n-type impurity into the first semiconductor layer without

passing through the first gate wiring;

second adding the n-type impurity into the first semiconductor layer through at least a portion of the first gate wiring; and

third adding a p-type impurity into the second semiconductor layer using the first gate wiring and the second gate wiring as masks;

wherein an angle between a side portion intersecting with the first semiconductor layer and the insulating film is in a range of 3 degrees to 60 degrees.

13. A semiconductor device comprising:

a semiconductor island on an insulating surface;

a channel region in the semiconductor island;

at least an LDD region being contact with the channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region;

a gate electrode being formed over the semiconductor island with a gate insulating film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate electrode,

wherein the first gate electrode has at least a taper portion and a flat portion,

wherein the first impurity region is overlapped with the taper portion of the first gate electrode with the gate insulating film interposed therebetween,

wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode.

14. A device according to claim 13, wherein an angle between the taper portion of the first gate electrode and the gate insulating film is in a range of 3 to 60 degrees.

15. A device according to claim 13, wherein the semiconductor island is a crystalline silicon island.

16. A device according to claim 13, wherein the first gate electrode includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while the second gate electrode includes at least one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), tungsten (W), or molybdenum (Mo), an n-type silicon containing phosphorus and silicide.

17. A device according to claim 13, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a rear-type projector, a front-type projector, a head mount display (a goggle-type display), a navigation system for vehicles, a personal computer, a mobile computer, a cellular phone, and an electronic book.

18. A semiconductor device comprising at least a CMOS transistor including an n-channel thin film transistor and a p-channel thin film transistor,

said n-channel thin film transistor including:

a first semiconductor island on an insulating surface;

a first channel region in the first semiconductor island;

at least a first LDD region being contact with the first channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region;

a gate electrode of the n-channel thin film transistor being formed over

the first semiconductor island with a gate insulating film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate electrode,

wherein the first gate electrode has at least a taper portion and a flat portion,

wherein the first impurity region is overlapped with the taper portion of the first gate electrode with the gate insulating film interposed therebetween,

wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode.

said p-channel thin film transistor including:

a second semiconductor island being formed on the insulating surface;

a second channel region in the second semiconductor island;

at least a fourth impurity region being formed in contact with the second channel region;

at least a fifth impurity region being formed in contact with the fourth impurity region;

a gate electrode of the p-channel thin film transistor being formed over the second channel region with the gate insulating film being interposed therebetween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein each of the fourth and fifth impurity regions is overlapped with neither the third gate electrode nor the fourth gate electrode.

19. A device according to claim 18, wherein an angle between the taper portion of the first gate electrode and the gate insulating film is in a range of 3 to 60 degrees.

20. A device according to claim 18, wherein each of the first and second semiconductor islands is a crystalline silicon island.

21. A device according to claim 18, wherein each of the first and third gate electrodes includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while each of the second and fourth gate electrodes includes at least one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), tungsten (W), or molybdenum (Mo), an n-type silicon containing phosphorus and silicide.

22. A device according to claim 18, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a rear-type projector, a front-type projector, a head mount display (a goggle-type display), a navigation system for vehicles, a personal computer, a mobile computer, a cellular phone, and an electronic book.

23. A semiconductor device comprising at least a CMOS transistor including an n-channel thin film transistor and a p-channel thin film transistor,

said n-channel thin film transistor including:

a first semiconductor island on an insulating surface;

a first channel region in the first semiconductor island;

at least a first LDD region being contact with the first channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region;

a gate electrode of the n-channel thin film transistor being formed over the first semiconductor island with a gate insulating film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate

electrode,

wherein the first gate electrode has at least a first taper portion and a first flat portion,

wherein the first impurity region is overlapped with the first taper portion of the first gate electrode with the gate insulating film interposed therebetween,

wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode.

said p-channel thin film transistor including:

a second semiconductor island being formed on the insulating surface;

a second channel region in the second semiconductor island;

at least a fourth impurity region being formed in contact with the second

a gate electrode of the p-channel thin film transistor being formed over the second channel region with the gate insulating film being interposed therebetween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein the third gate electrode has at least a second taper portion and a second flat portion,

wherein the fourth impurity region is overlapped with neither the third gate electrode nor the fourth gate electrode.

24. A device according to claim 23, wherein each of angles between the first taper portion of the first gate electrode and the gate insulating film and between the second taper portion of the third gate electrode and the gate insulating film is in a range of 3 to 60 degrees.

25. A device according to claim 23, wherein each of the first and second semiconductor islands is a crystalline silicon island.

26. A device according to claim 23, wherein each of the first and third gate electrodes includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while each of the second and fourth gate electrodes includes at least one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), tungsten (W), or molybdenum (Mo), an n-type silicon containing phosphorus and silicide.

27. A device according to claim 23, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a rear-type projector, a front-type projector, a head mount display (a goggle-type display), a navigation system for vehicles, a personal computer, a mobile computer, a cellular phone, and an electronic book.

28. A semiconductor device comprising at least a CMOS transistor including an n-channel thin film transistor and a p-channel thin film transistor,

said n-channel thin film transistor including:

a first semiconductor island on an insulating surface;

a first channel region in the first semiconductor island;

at least a first LDD region being contact with the first channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region;

a gate electrode of the n-channel thin film transistor being formed over the first semiconductor island with a gate insulating film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate

electrode,

wherein the first gate electrode has at least a taper portion and a flat portion,

wherein the first impurity region is overlapped with the taper portion of the first gate electrode with the gate insulating film interposed therebetween,

wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode.

said p-channel thin film transistor including:

a second semiconductor island being formed on the insulating surface;

a second channel region in the second semiconductor island;

at least a fourth impurity region being formed in contact with the second

a gate electrode of the p-channel thin film transistor being formed over the second channel region with the gate insulating film being interposed therebetween having a third gate electrode and a fourth gate electrode being formed on the third gate electrode,

wherein the fourth impurity region is overlapped with neither the third gate electrode nor the fourth gate electrode.

29. A device according to claim 28, wherein an angle between the taper portion of the first gate electrode and the gate insulating film is in a range of 3 to 60 degrees.

30. A device according to claim 28, wherein each of the first and second semiconductor islands is a crystalline silicon island.

31. A device according to claim 28, wherein each of the first and third gate electrodes includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while each of the second and fourth gate electrodes includes at least

one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), tungsten (W), or molybdenum (Mo), an n-type silicon containing phosphorus and silicide.

32. A device according to claim 28, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a rear-type projector, a front-type projector, a head mount display (a goggle-type display), a navigation system for vehicles, a personal computer, a mobile computer, a cellular phone, and an electronic book.

33. An electroluminescence display device comprising:

a pixel portion and a peripheral driving circuit portion over a substrate;

at least a first thin film transistor for controlling a current and a second thin film transistor for switching each being formed in the pixel portion;

at least a CMOS transistor being formed in the peripheral driving circuit portion;

said first thin film transistor comprising:

a semiconductor island on an insulating surface;

a channel region in the semiconductor island;

at least an LDD region being contact with the channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region;

a gate electrode being formed over the semiconductor island with a gate insulating film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate electrode,

wherein the first gate electrode has at least a taper portion and a flat portion,

wherein the first impurity region is overlapped with the taper portion of the first gate electrode with the gate insulating film interposed therebetween,

wherein the second impurity region is overlapped with neither the first gate electrode nor the second gate electrode,

a pixel electrode being electrically connected to the third impurity region of the first thin film transistor;

a light emitting layer being formed over the pixel electrode;

an electrode being formed over the light emitting layer.

34. A device according to claim 33, wherein an angle between the taper portion of the first gate electrode and the gate insulating film is in a range of 3 to 60 degrees.

35. A device according to claim 33, wherein the semiconductor island is a crystalline silicon island.

36. A device according to claim 33, wherein the first gate electrode includes at least one selected from the group consisting of chromium (Cr), tantalum (Ta) an n-type silicon containing phosphorus, titanium (Ti), tungsten (W), and molybdenum (Mo) while the second gate electrode includes at least one selected from the group consisting of aluminum (Al), copper (Cu), chromium (Cr), tantalum (Ta), titanium (Ti), tungsten (W), or molybdenum (Mo), an n-type silicon containing phosphorus and silicide.

37. The electroluminescence display device of claim 33 in combination with one selected from the group consisting of a video camera, a digital camera, a rear-type projector, a front-type projector, a head mount display (a goggle-type display), a navigation system for vehicles, a personal computer, a mobile computer, a cellular phone,

and an electronic book.

38. A device according to claim 33, wherein the light emitting layer is an EL layer.

39. A device according to claim 33, wherein a drain region of the second thin film transistor is electrically connected to the gate electrode of the first thin film transistor.

40. A device according to claim 33, wherein the second thin film transistor has a multi-gate structure.

41. A device according to claim 33, wherein at least one of the pixel electrode and the electrode is transparent.